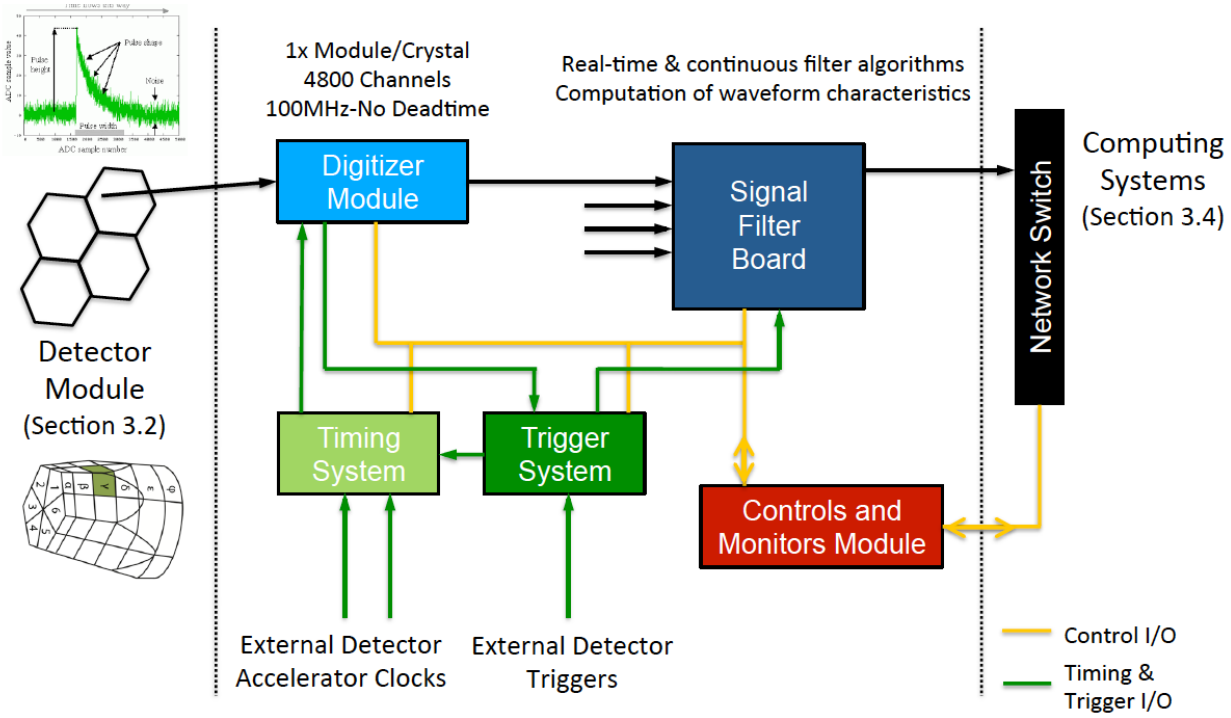
GRETA Electronics Summary



Digitizer Module – Full analog to digital streamer

IN GRETA Clock + Analog preamplifier signals in for 36 segments + 1 core
Segment ADCs: 2/4 channels per chip, low-power
Core ADCs: Multiple ADCs to optimize linearity and cover range (<25MeV)
OUT Waveform data stream (~64Gbits/sec) on fiber
OUT Fast trigger (<500 ns) + slow trigger data stream

Focus: ADC Range and Fast Trigger

Signal Filter Board – Raw waveforms to "Mode 3" events

IN Waveform data stream and Trigger decisions
FPGA 20 μs trigger latency allowed, buffering to eliminate dead time
OUT At least 4k trigger-selected events/sec, sent by UDP
37 segments + core: energy + timing filters and windowed waveforms

Timing System – GRETA timestamp clock source

IN External clocks for labeling data in additional timestamp domains
OUT Clock ticks and Sync

Trigger System – Physics event selector

IN 120 Digitizer trigger-data streams
IN External triggers, formats to be decided, e.g. NIM pulse
Trigger primitives (values considered in trigger algorithms):
Crystal multiplicity, external detector, fast (~1μs) energy, hit pattern
OUT Timestamped trigger decisions
OUT Trigger details (times, hit patterns, energies) possibly useful in Decomp